16-Bit, 170/200-MSPS Analog-to-Digital Converters

FEATURES

- **170/200-MSPS Sample Rates**
- **16-Bit Resolution, 78 dBFS Noise Floor**
- **SFDR = 95 dBc**
- **On-Chip High Impedance Analog Buffer**
- **Efficient DDR LVDS-Compatible Outputs**
- **Power-Down Mode: 70 mW**
- **Pin-for-Pin with ADS5483/5482/5481, 135/105/80-MSPS ADCs**
- **QFN-64 PowerPAD™ Package (9 mm × 9 mm footprint)**
- **Industrial Temperature Range: –40°C to 85°C**

APPLICATIONS

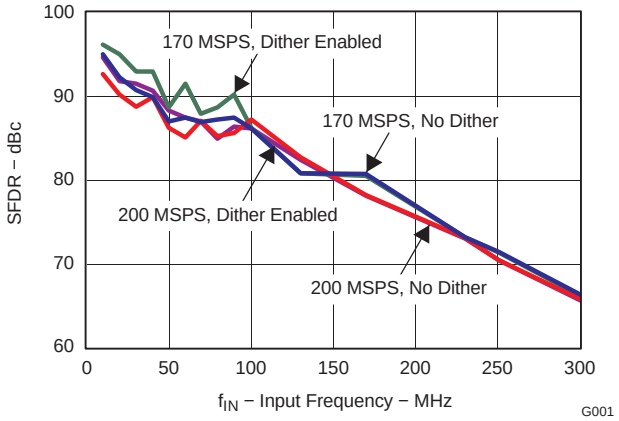
- **Wireless Infrastructure**
- **Test and Measurement Instrumentation**
- **Software-Defined Radio**
- **Data Acquisition**
- **Power Amplifier Linearization**
- **Radar**
- **Medical Imaging**

DESCRIPTION

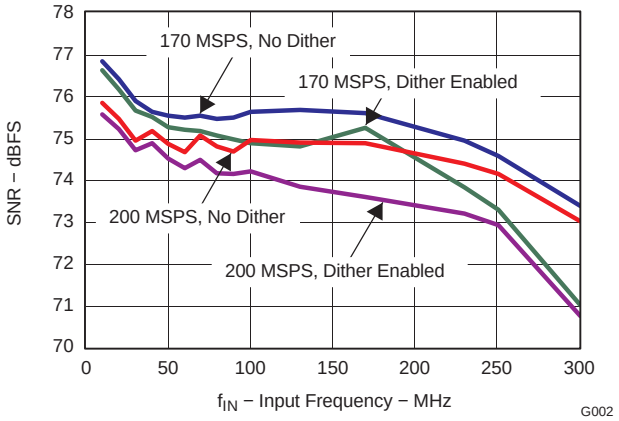
The ADS5484/ADS5485 (ADS548x) is a 16-bit family of analog-to-digital converters (ADCs) that operate from both a 5-V supply and 3.3-V supply while providing LVDS-compatible digital outputs. The ADS548x integrated analog input buffer isolates the internal switching of the onboard track and hold (T & H) from disturbing the signal source while providing a high-impedance input. An internal reference generator is provided to simplify the system design. Internal dither is available to improve SFDR. These devices are drop-in compatible to the ADS5483/5482/5481, creating a pin-compatible family from 80 – 200 MSPS. Designed for highest total ENOB, the ADS548x family has outstanding low noise performance and spurious-free dynamic range.

The ADS548x family is available in a QFN-64 PowerPAD package. The devices are built on Texas Instruments complementary bipolar process (BiCom3) and are specified over the full industrial temperature range (–40°C to 85°C).

SFDR vs INPUT FREQUENCY

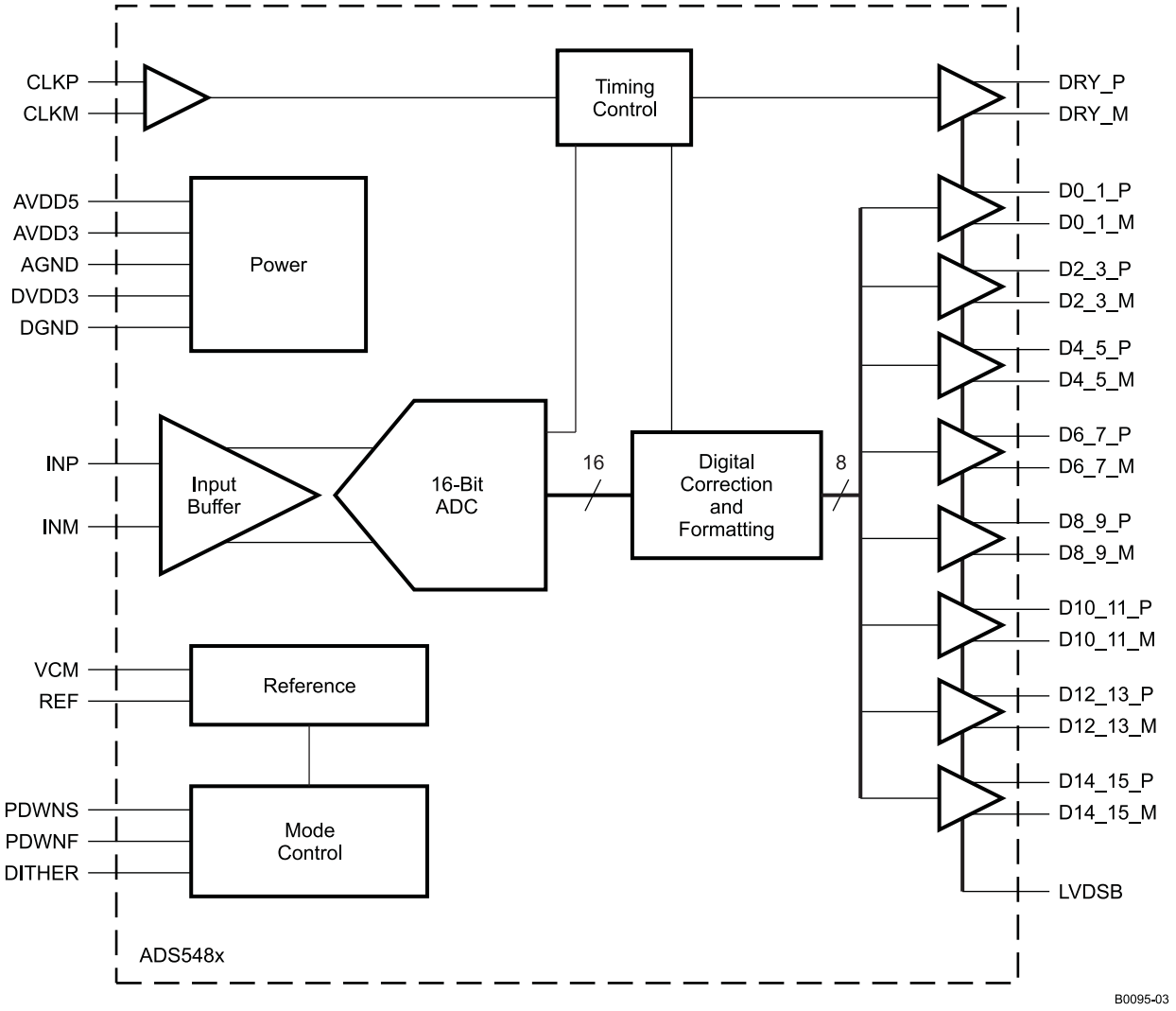


SNR vs INPUT FREQUENCY



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5484	QFN-64	RGC	–40°C to 85°C	AZ5484	ADS5484IRGCT	Tape and reel, 250
					ADS5484IRGCR	Tape and reel, 2000
ADS5485	QFN-64	RGC	–40°C to 85°C	AZ5485	ADS5485IRGCT	Tape and reel, 250
					ADS5485IRGCR	Tape and reel, 2000

(1) For the most current product and ordering information see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com..

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		ADS5484, ADS5485	UNIT
Supply voltage	AVDD5 to GND	6	V
	AVDD3 to GND	5	V
	DVDD3 to GND	5	V
Analog input to GND	Valid when AVDD5 is within normal operating range. When AVDD5 is off, analog inputs should be < 0.5 V. If not, the protection diode between the inputs and AVDD5 becomes forward-biased and could be damaged or shorten device lifetime (see Figure 30). Short transient conditions during power on/off are not a concern.	–0.3 to (AVDD5 + 0.3)	V
Clock input to GND	Valid when AVDD3 is within normal operating range. When AVDD3 is off, clock inputs should be < 0.5 V. If not, the protection diode between the inputs and AVDD3 becomes forward-biased and could be damaged or shorten device lifetime (see Figure 37). Short transient conditions during power on/off are not a concern.	–0.3 to (AVDD3 + 0.3)	V
CLKP to CLKM		±2.5	V
Digital data output to GND		–0.3 to (DVDD3 + 0.3)	V
Digital data output plus-to-minus		±1	V
Operating temperature range		–40 to 85	°C
Maximum junction temperature		150	°C
Storage temperature range		–65 to 150	°C
ESD, human-body model (HBM)		2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. Kirkendall voidings and current density information for calculation of expected lifetime are available upon request.

THERMAL CHARACTERISTICS(1)

PARAMETER	TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$	Soldered thermal pad, no airflow	20	°C/W
	Soldered thermal pad, 150-LFM airflow	16	
$R_{\theta JC}$	Thermal resistance from the junction to the package case (top)	7	
$R_{\theta JP}$	Thermal resistance from the junction to the thermal pad (bottom)	0.2	

(1) Using 49 thermal vias (7 × 7 array). See *PowerPAD Package* in the Application Information section.

RECOMMENDED OPERATING CONDITIONS

		ADS5484, ADS5485			UNIT
		MIN	NOM	MAX	
SUPPLIES					
AVDD5	Analog supply voltage	4.75	5	5.25	V
AVDD3	Analog supply voltage	3.15	3.3	3.45	V
DVDD3	Output driver supply voltage	3	3.3	3.6	V
ANALOG INPUT					
	Differential input voltage range		3		V_{PP}
VCM	Input common-mode voltage		3.1		V
DIGITAL OUTPUT (DRY, DATA)					
	Maximum differential output load (parasitic or intentional)		5		pF
	Differential output resistance		100		Ω
CLOCK INPUT (CLK)					
	CLK input sample rate (sine wave)	10		Max Rated Clock	MSPS
	Clock amplitude, differential sine wave (see Figure 39)	1.5		5	V_{PP}
	Clock duty cycle (see Figure 44)	45%	50%	55%	
T_A	Operating free-air temperature	–40		+85	°C

ELECTRICAL CHARACTERISTICS (ADS5484, ADS5485)

Typical values at T_A = 25°C: minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = max rated, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS5484			ADS5485			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Clock rate				170			200	MSPS
	Resolution				16			16	Bits
ANALOG INPUTS									
	Differential input voltage range			3			3		V_{PP}
	Analog input common-mode voltage	Self-biased; see VCM specification below		3.1			3.1		V
	Input resistance (dc)	Each input to VCM		1000			1000		Ω
	Input capacitance	Each input to GND (unsoldered package)		3.5			3.5		pF
	Analog input bandwidth (–3dB)			730			730		MHz
CMRR	Common-mode rejection ratio	Common-mode signal 70 MHz (see Figure 26)		65			65		dB
INTERNAL REFERENCE VOLTAGE									
VREF	Reference voltage	With internal voltage reference		1.2			1.2		V
VCM	Analog input common-mode voltage reference output		2.9	3.1	3.3	2.9	3.1	3.3	V
	VCM temperature coefficient			-1			-1		mV/°C

ELECTRICAL CHARACTERISTICS (ADS5484, ADS5485) (continued)

Typical values at T_A = 25°C: minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = max rated, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted.

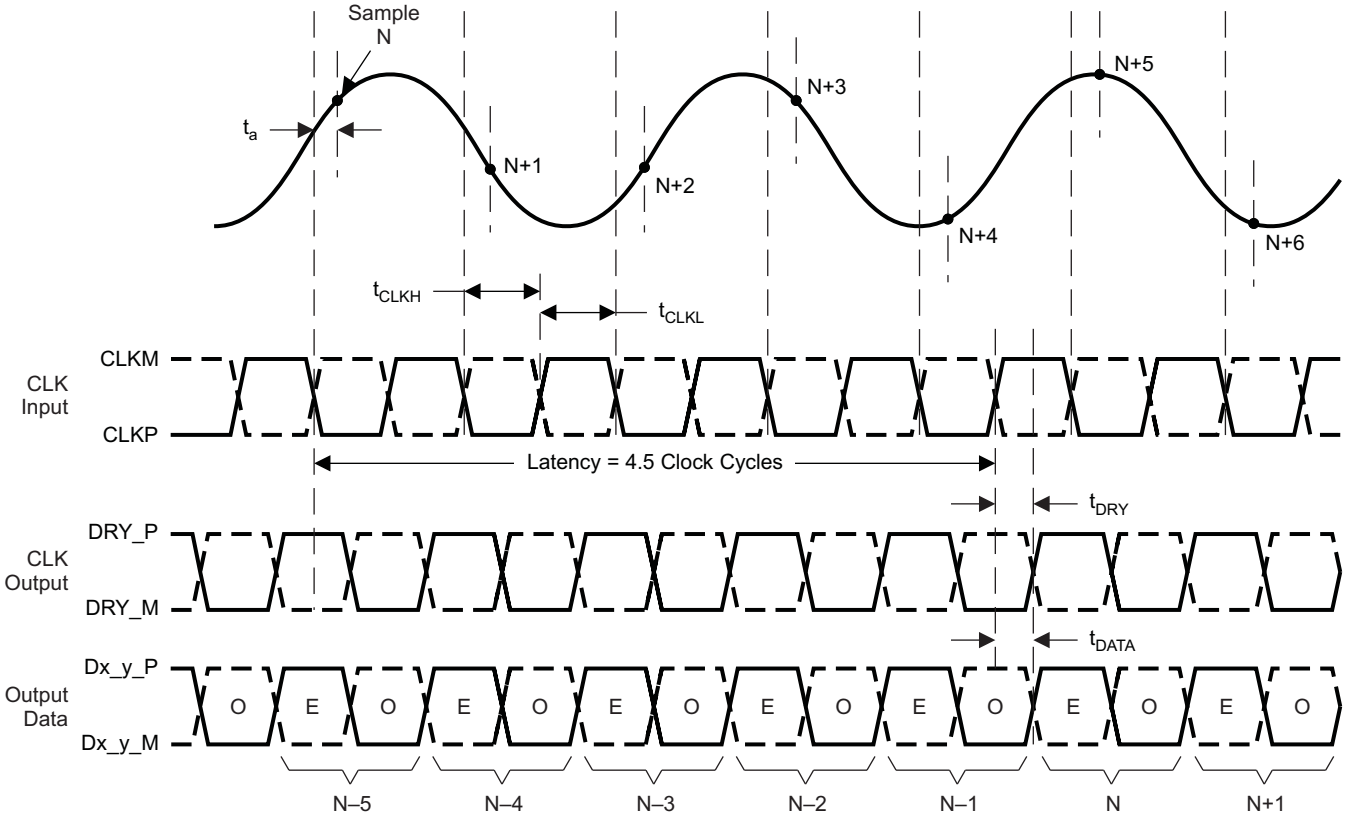
PARAMETER		TEST CONDITIONS	ADS5484			ADS5485			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC ACCURACY									
DNL	Differential nonlinearity error	No missing codes, f_{IN} = 30 MHz	-0.99	±0.5	1.0	-0.99	±0.5	1.0	LSB
INL	Integral nonlinearity error	f_{IN} = 30 MHz	-10	±3	+10	-10	±3	+10	LSB
	Offset error		-15		15	-15		15	mV
	Offset temperature coefficient			-0.02			-0.02		mV/°C
	Gain error		-6	±2	6	-6	±2	6	%FS
	Gain temperature coefficient			-0.01			-0.01		mV/°C
POWER SUPPLY									
I_{AVDD5}	5-V analog current	V_{IN} = Full-scale, f_{IN} = 30 MHz, f_S = Max rated, Normal operation		310	330		310	330	mA
I_{AVDD3}	3.3-V analog current			126	150		126	150	mA
I_{DVDD3}	3.3-V digital/LVDS current			60	65		60	65	mA
	Total power dissipation			2.16	2.35		2.16	2.35	W
I_{AVDD5}	5-V analog current	Light sleep mode (PDWNF = H, PDWNS = L)		98			98		mA
I_{AVDD3}	3.3-V analog current			35			35		mA
I_{DVDD3}	3.3-V digital/LVDS current			0.07			0.07		mA
	Total power dissipation			600	680		600	680	mW
I_{AVDD5}	5-V analog current	Deep sleep mode (PDWNF = L, PDWNS = H)		13			13		mA
I_{AVDD3}	3.3-V analog current			1			1		mA
I_{DVDD3}	3.3-V digital/LVDS current			0.07			0.07		mA
	Total power dissipation			70	100		70	100	mW
	Fast wake-up time (light sleep)	From PDWNF disabled		600			600		µS
	Slow wake-up time (deep sleep)	From PDWNS disabled		6			6		mS
PSRR	AVDD5 supply	Power-supply rejection ratio, Without 0.1-µF board supply capacitors, with 1-MHz supply noise (see Figure 46)		60			60		dB
	AVDD3 supply			80			80		dB
	DVDD3 supply			95			95		dB
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio, dither disabled	f_{IN} = 10 MHz	75	76.8		73.5	75.8		dBFS
		f_{IN} = 30 MHz	74.5	75.9		73	75		
		f_{IN} = 70 MHz		75.7			75		
		f_{IN} = 130 MHz	73.5	75.7		72	74.8		
		f_{IN} = 170 MHz		75.6			74.8		
		f_{IN} = 230 MHz		74.9			74.4		
SFDR	Spurious-free dynamic range, dither disabled	f_{IN} = 10 MHz	84	95		84	93		dBc
		f_{IN} = 30 MHz	84	91		82	90		
		f_{IN} = 70 MHz		87			87		
		f_{IN} = 130 MHz	78	86		78	85		
		f_{IN} = 170 MHz		81			78		
		f_{IN} = 230 MHz		73			73		
HD2	Second-harmonic, dither disabled	f_{IN} = 10 MHz	84	100		84	100		dBc
		f_{IN} = 30 MHz	84	95		82	95		
		f_{IN} = 70 MHz		95			95		
		f_{IN} = 130 MHz	78	87		78	85		
		f_{IN} = 170 MHz		81			78		
		f_{IN} = 230 MHz		73			73		

ELECTRICAL CHARACTERISTICS (ADS5484, ADS5485) (continued)

Typical values at T_A = 25°C: minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = max rated, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS5484			ADS5485			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
HD3	Third-harmonic, dither disabled	f_{IN} = 10 MHz	84	97		84	99		dBc
		f_{IN} = 30 MHz	84	91		82	87		
		f_{IN} = 70 MHz		87			87		
		f_{IN} = 130 MHz	78	86		78	85		
		f_{IN} = 170 MHz		82			81		
		f_{IN} = 230 MHz		73			73		
	Worst harmonic/spur (other than HD2 and HD3), dither disabled	f_{IN} = 10 MHz	84	96		84	93		dBc
		f_{IN} = 30 MHz	84	91		82	90		
		f_{IN} = 70 MHz		90			90		
		f_{IN} = 130 MHz	78	91		78	90		
		f_{IN} = 170 MHz		90			90		
		f_{IN} = 230 MHz		87			87		
THD	Total harmonic distortion, dither disabled	f_{IN} = 10 MHz	81	92		81	92		dBc
		f_{IN} = 30 MHz	81	86		79	85		
		f_{IN} = 70 MHz		86			85		
		f_{IN} = 130 MHz	75	84		75	81		
		f_{IN} = 170 MHz		78			76		
		f_{IN} = 230 MHz		70			70		
SINAD	Signal-to-noise and distortion, dither disabled	f_{IN} = 10 MHz	73.5	75.8		71.5	74.6		dBc
		f_{IN} = 30 MHz	73	75		71	73.8		
		f_{IN} = 70 MHz		74.3			73.7		
		f_{IN} = 130 MHz	71.5	73.8		70	72.9		
		f_{IN} = 170 MHz		72.9			71.7		
		f_{IN} = 230 MHz		68.7			68.4		
IMD	Two-tone SFDR (worst spurious or IMD)	f_{IN1} = 29.5 MHz, f_{IN2} = 30.5 MHz, Each at –7 dBFS		99.1			95.9		dBFS
		f_{IN1} = 69.5 MHz, f_{IN2} = 70.5 MHz, Each at –10 dBFS		95.3			95.2		
ENOB	Effective number of bits	f_{IN} = 10 MHz (from SINAD in dBc at -1dBFS)	11.92	12.3		11.58	12.1		Bits
Noise	RMS idle-channel noise	Analog inputs shorted together		2.9			2.9		LSB rms
				78			78		dBFS
LVDS DIGITAL OUTPUTS									
V_{OD}	Differential output voltage (±)	Assumes a 100-Ω differential load on each LVDS pair and LVDS bias = 3.5 mA	247	350	454	247	350	454	mV
V_{OC}	Common-mode output voltage		1.125	1.25	1.375	1.125	1.25	1.375	V
DIGITAL INPUTS									
V_{IH}	High-level input voltage	PDWNF, PDWNS, DITHER	2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IH}	High-level input current				1			1	µA
I_{IL}	Low-level input current		-1			-1			µA
	Input capacitance			2			2		pF

TIMING INFORMATION



E = Even Bits = B0, B2, B4, B6, B8, B10, B12, B14
O = Odd Bits = B1, B3, B5, B7, B9, B11, B13, B15

T0158-02

Figure 1. Timing Diagram

TIMING CHARACTERISTICS(1)

Typical values at T_A = 25°C: minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = max rated, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay			200		ps
	Aperture jitter, rms	Internal jitter of the ADC		80		fs
	Latency			4.5		cycles
t_{CLK}	Clock period	CLK = max rated clock for that part number	1e9/CLK		100	ns
t_{CLKH}	Clock pulse duration, high		0.5e9/CLK		50	ns
t_{CLKL}	Clock pulse duration, low		0.5e9/CLK		50	ns
t_{DRY}	CLK to DRY delay time(2)	Zero crossing, 5-pF parasitic to GND	800	1250	1700	ps
t_{DATA}	CLK to DATA delay time(2)		700	1250	1800	ps
t_{SKEW}	DATA to DRY skew	t_{DATA} – t_{DRY}, 5-pF parasitic to GND	–500	0	500	ps
t_{RISE}	DRY/DATA rise time	5-pF parasitic to GND		500		ps
t_{FALL}	DRY/DATA fall time			500		ps

(1) Timing parameters are assured by design or characterization, but not production tested.
(2) DRY and DATA are updated on the rising edge of CLK input. The latency must be added to t_{DATA} to determine the overall propagation delay.

PIN CONFIGURATION

ADS548x
RGC Package
(Top View)

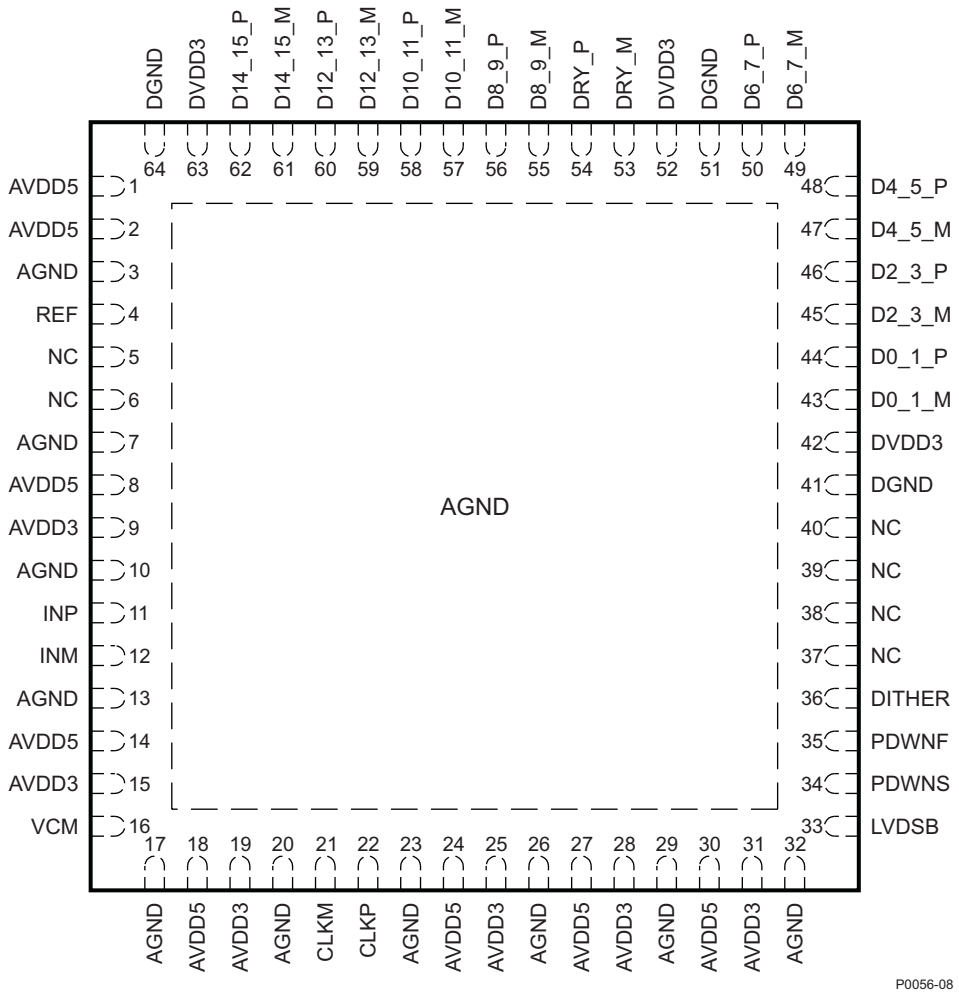


Table 1. PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
AVDD5	1, 2, 8, 14, 18, 24, 27, 30	5-V analog supply
AVDD3	9, 15, 19, 25, 28, 31	3.3-V analog supply
AGND	3, 7, 10, 13, 17, 20, 23, 26, 29, 32	Analog ground
DVDD3	42, 52, 63	3.3-V digital supply
DGND	41, 51, 64	Digital ground
NC	5, 6, 37-40	No connect - leave floating
INP, INM	11, 12	Differential analog inputs (P = plus = true, M = minus = complement)
CLKM, CLKP	21, 22	Differential clock inputs (P = plus = true, M = minus = complement)
REF	4	Reference voltage input/output (1.2 V nominal). To use an external reference and to turn the internal reference off, pull both PDWNF and PDWNS to logic high (DVDD3). A 0.1-µF capacitor to ground on REF is recommended but not required.
VCM	16	Analog input common mode, output (3.1V), for use in applications that require use of the internally generated common-mode. See the Applications section for more information on using VCM. A 0.1-µF capacitor to ground on VCM is recommended but not required.
LVDSB	33	External bias resistor for LVDS bias current, normally 10 kΩ to GND to provide nominal 3.5-mA LVDS current.
PDWNF	35	Light sleep power down, fast wake-up, logic high (DVDD3) = light sleep enabled (bandgap reference remains on)
PDWNS	34	Deep sleep power down, slow wake-up, logic high (DVDD3) = deep sleep enabled (bandgap reference is off)
DITHER	36	Dither enable, logic high (DVDD3) = dither enabled
DRY_P, DRY_M	54, 53	Data ready signal (LVDS clock out) (P = plus = true, M = minus = complement)
D14_15_P, D14_15_M	62, 61	DDR LVDS output bits 14 then 15 (15 is MSB) (P = plus = true, M = minus = complement)
DE_O_P, DE_O_M	43-50, 55-62	DDR LVDS output bits E (even) then O (odd) (P = plus = true, M = minus = complement)
D0_1_P, D0_1_M	44, 43	DDR LVDS output bits 0 then 1 (0 is LSB) (P = plus = true, M = minus = complement)
PowerPAD	65	Analog ground (exposed pad on bottom of package)

TYPICAL CHARACTERISTICS

At T_A = 25°C, sampling rate = max rated, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

ADS5484 - 170-MSPS Typical Data

Plots in this section are with a clock of 170 MSPS, unless otherwise specified.

ADS5484 SPECTRAL PERFORMANCE vs FFT for 10-MHz INPUT SIGNAL

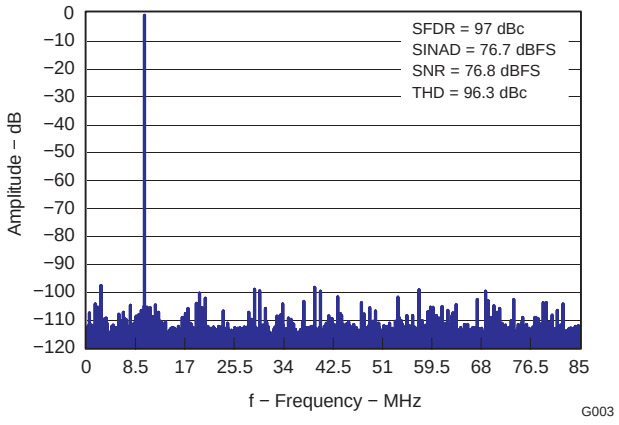


Figure 2.

ADS5484 SPECTRAL PERFORMANCE vs FFT for 70-MHz INPUT SIGNAL

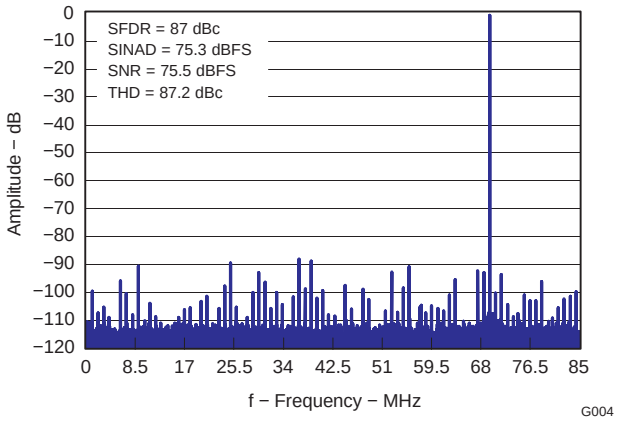


Figure 3.

ADS5484 SPECTRAL PERFORMANCE vs FFT for 130-MHz INPUT SIGNAL

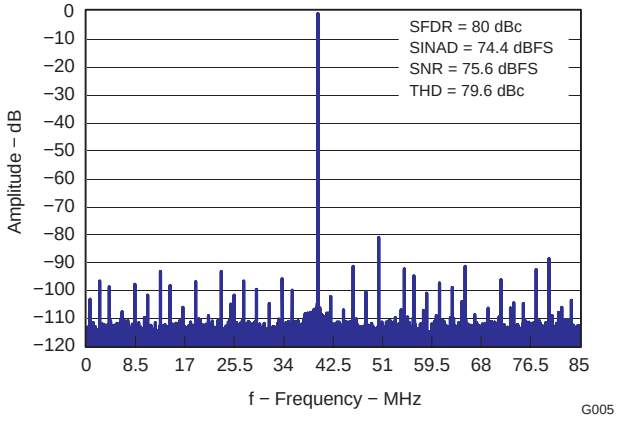


Figure 4.

ADS5484 SPECTRAL PERFORMANCE vs FFT for 230-MHz INPUT SIGNAL

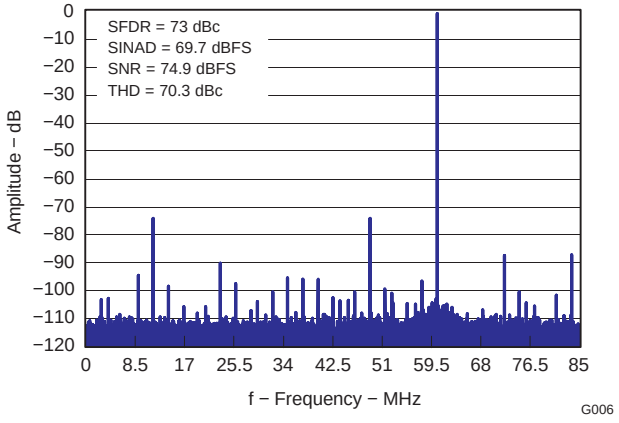


Figure 5.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, sampling rate = max rated, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

ADS5484 DIFFERENTIAL NONLINEARITY

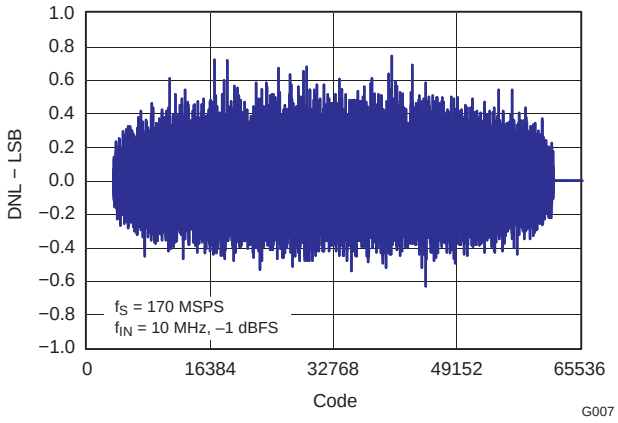


Figure 6.

ADS5484 INTEGRAL NONLINEARITY

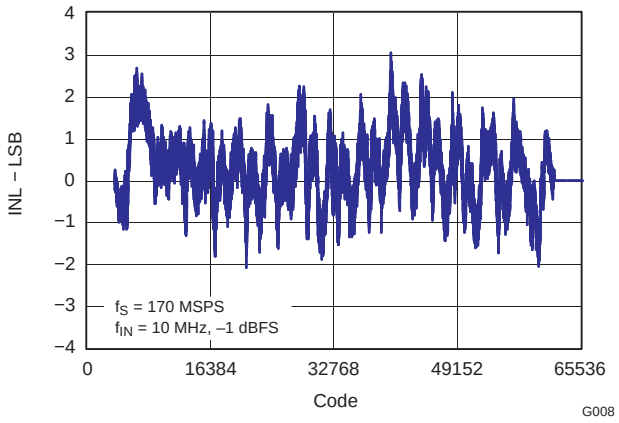


Figure 7.

ADS5484 AC PERFORMANCE vs INPUT AMPLITUDE (130-MHz Input Signal)

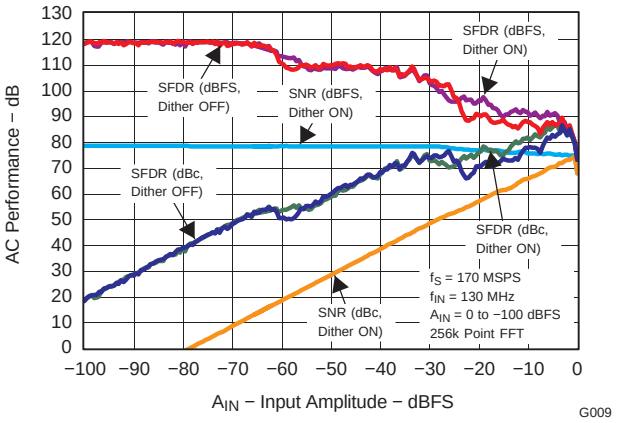


Figure 8.

ADS5484 AC PERFORMANCE vs INPUT AMPLITUDE (130-MHz Input Signal)

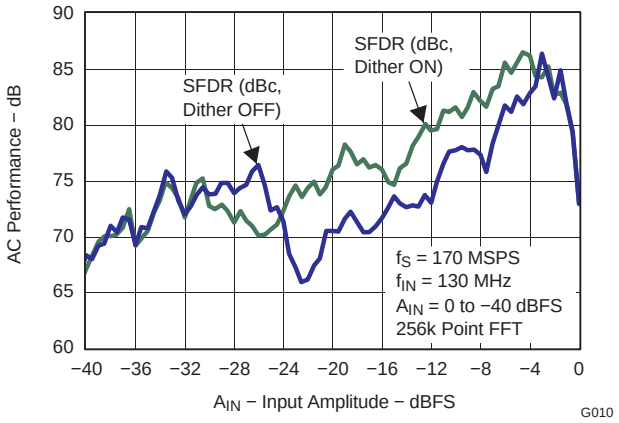


Figure 9.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, sampling rate = max rated, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

ADS5484 TWO-TONE PERFORMANCE vs INPUT AMPLITUDE (f_1 = 69.5 MHz and f_2 = 70.5 MHz)

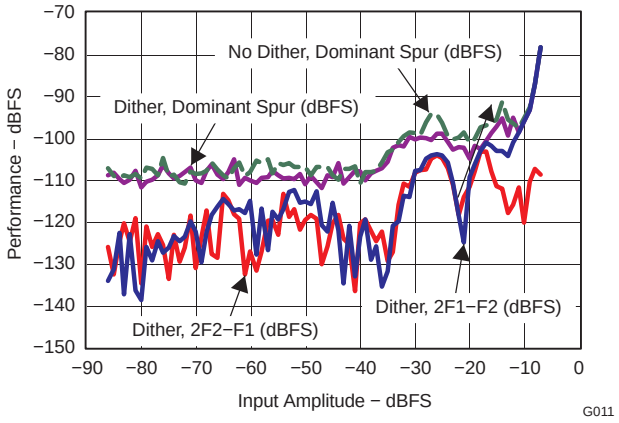


Figure 10.

ADS5484 30-MHz SFDR vs AVDD5 and AVDD3 OVER TEMPERATURE

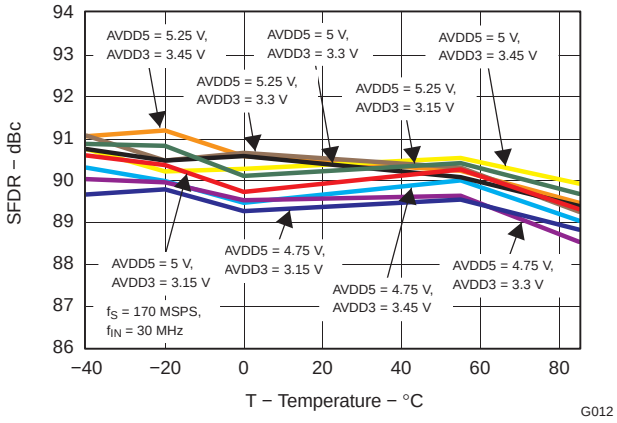


Figure 11.

ADS5484 30-MHz SNR vs AVDD5 and AVDD3 OVER TEMPERATURE

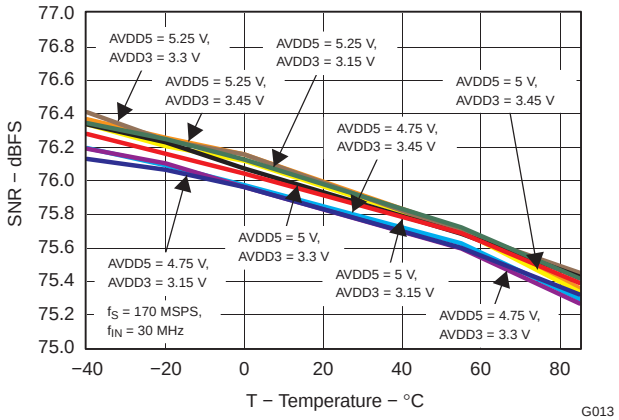


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, sampling rate = max rated, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

ADS5485 - 200-MSPS Typical Data

Plots in this section are with a clock of 200 MSPS, unless otherwise specified.

ADS5485 SPECTRAL PERFORMANCE vs FFT for 10-MHz INPUT SIGNAL

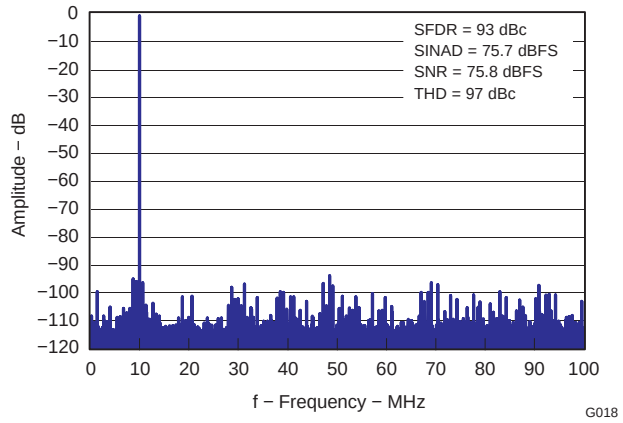


Figure 13.

ADS5485 SPECTRAL PERFORMANCE vs FFT for 70-MHz INPUT SIGNAL

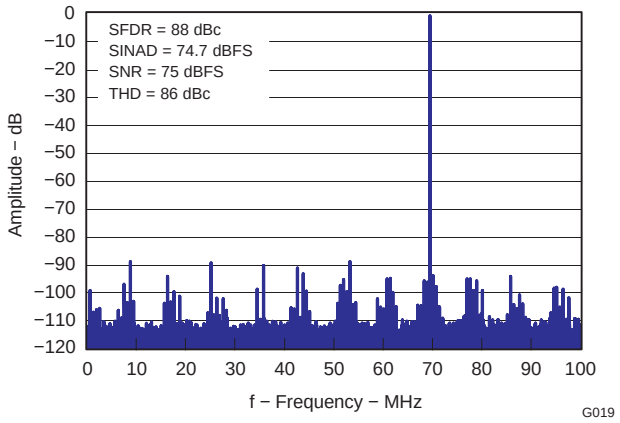


Figure 14.

ADS5485 SPECTRAL PERFORMANCE vs FFT for 130-MHz INPUT SIGNAL

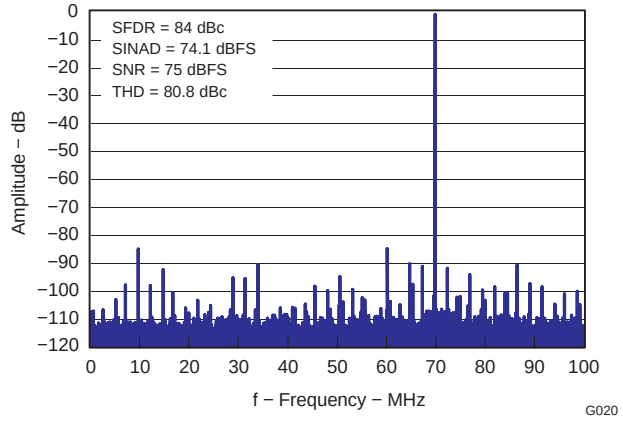


Figure 15.

ADS5485 SPECTRAL PERFORMANCE vs FFT for 230-MHz INPUT SIGNAL

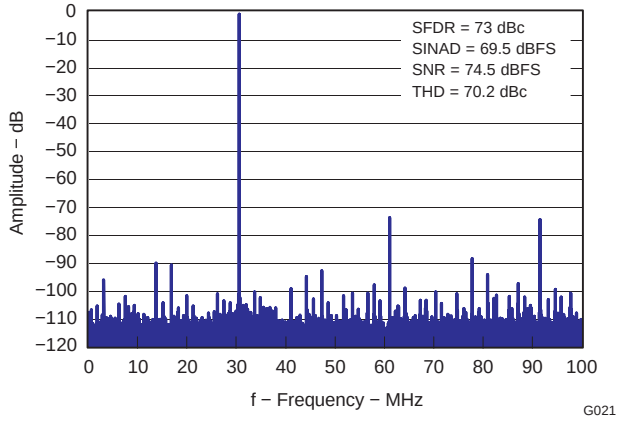


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, sampling rate = max rated, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

ADS5485 DIFFERENTIAL NONLINEARITY

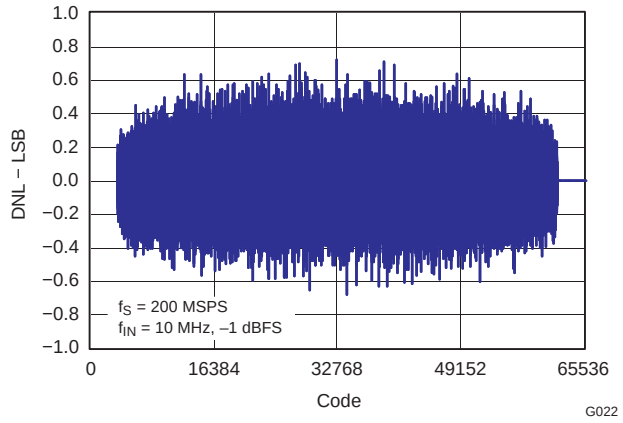


Figure 17.

ADS5485 INTEGRAL NONLINEARITY

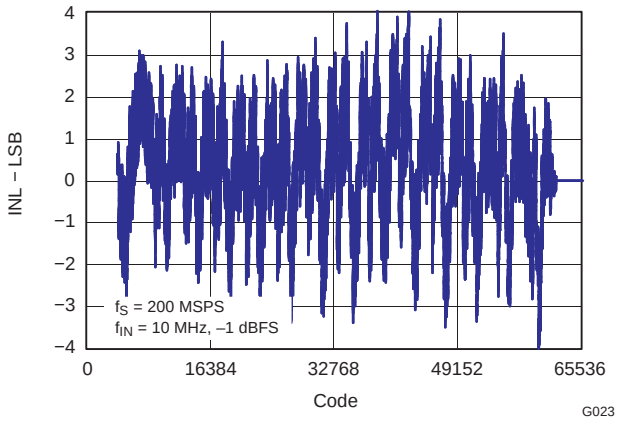


Figure 18.

ADS5485 AC PERFORMANCE vs INPUT AMPLITUDE (130-MHz Input Signal)

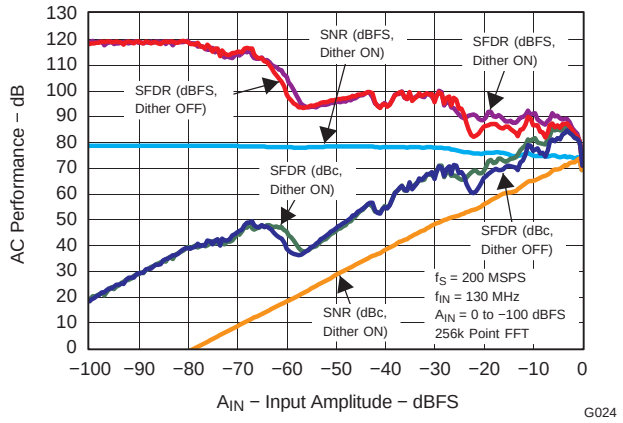


Figure 19.

ADS5485 AC PERFORMANCE vs INPUT AMPLITUDE (130-MHz Input Signal)

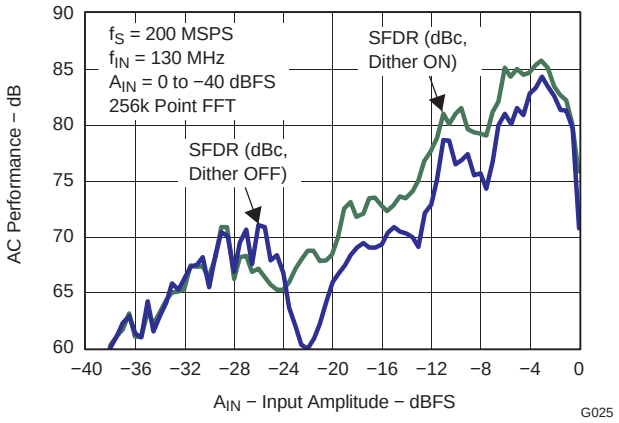


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, sampling rate = max rated, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

ADS5485 TWO-TONE PERFORMANCE vs INPUT AMPLITUDE (f_1 = 69.5 MHz and f_2 = 70.5 MHz)

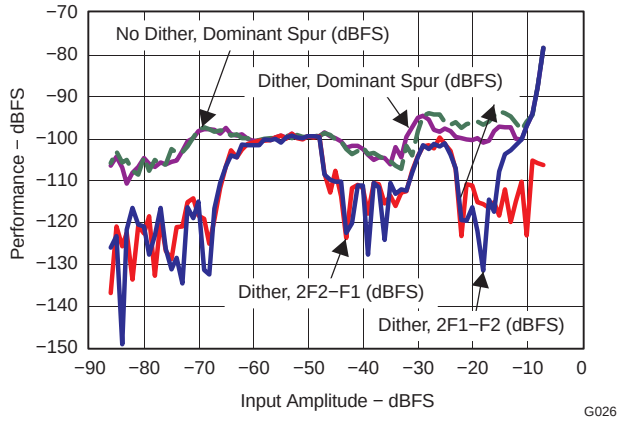


Figure 21.

ADS5485 30-MHz SFDR vs AVDD5 and AVDD3 OVER TEMPERATURE

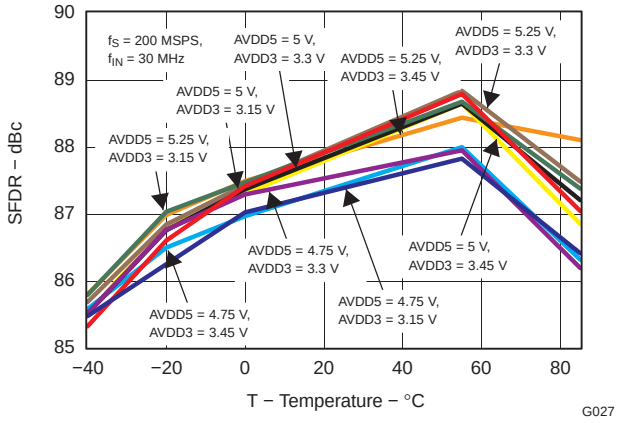


Figure 22.

ADS5485 30-MHz SNR vs AVDD5 and AVDD3 OVER TEMPERATURE

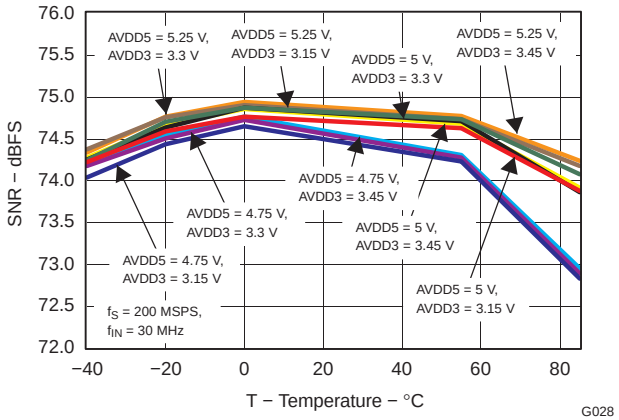


Figure 23.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, sampling rate = max rated, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

Typical Data, Valid for Both ADS5484/5485

Plots in this section are valid for either device or otherwise have combined plots.

NORMALIZED GAIN RESPONSE vs INPUT FREQUENCY

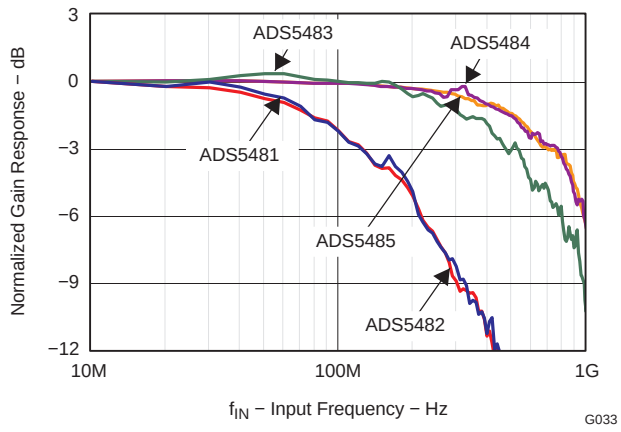


Figure 24.

NOISE HISTOGRAM WITH INPUTS SHORTED

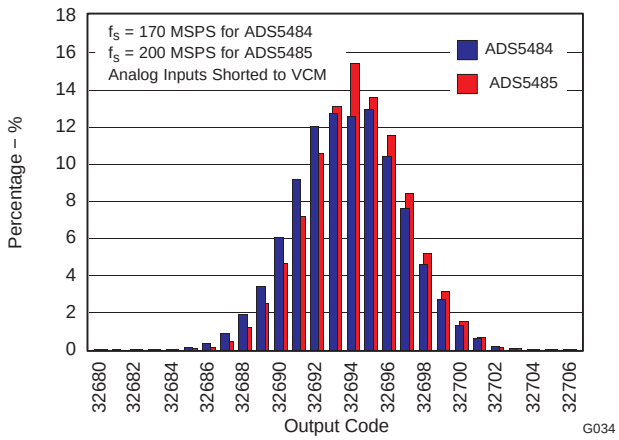


Figure 25.

CMRR vs COMMON-MODE INPUT FREQUENCY

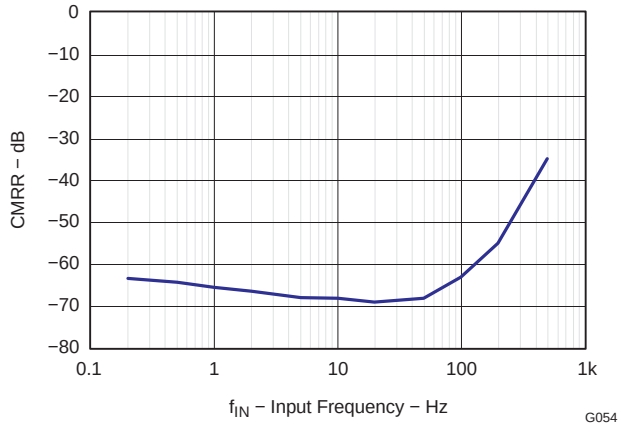


Figure 26.

ADC WAKE-UP TIME

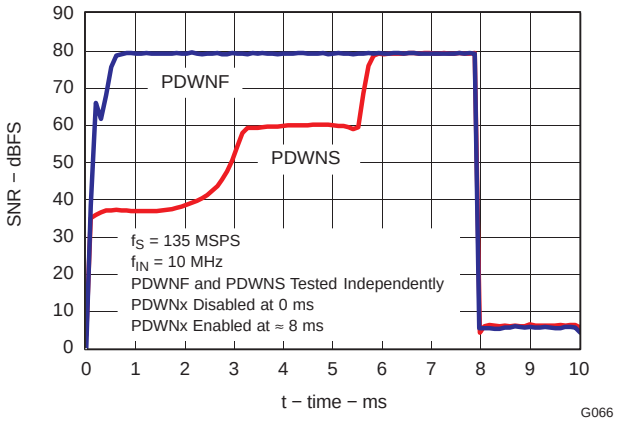


Figure 27.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, sampling rate = max rated, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

SNR vs INPUT FREQUENCY AND SAMPLING FREQUENCY

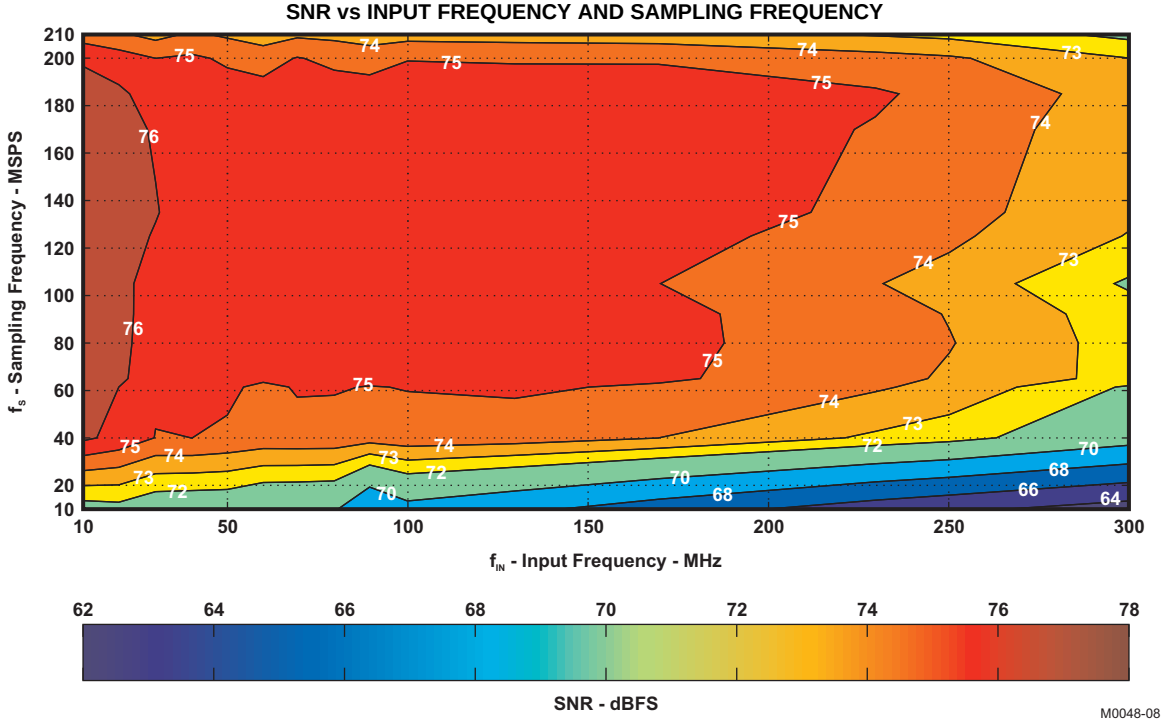


Figure 28.

SFDR vs INPUT FREQUENCY AND SAMPLING FREQUENCY

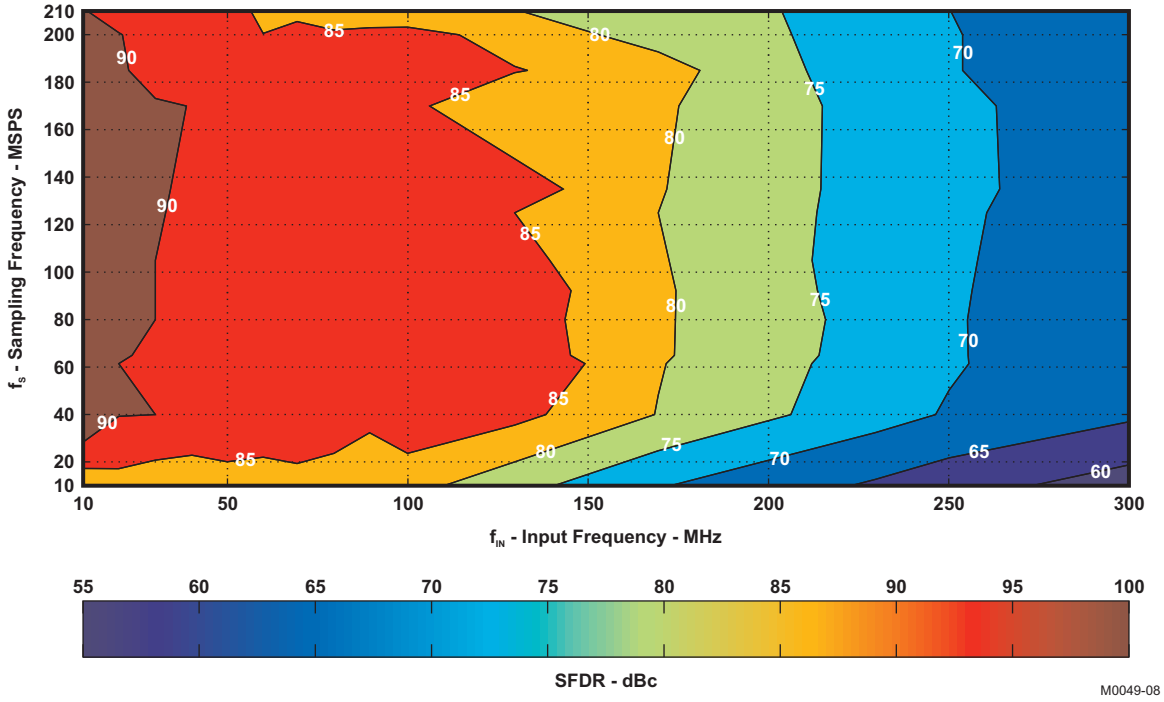


Figure 29.

APPLICATIONS INFORMATION

Theory of Operation

The ADS5484/ADS5485 (ADS548x) is a 16-bit, 170/200-MSPS family of monolithic pipeline ADCs. The bipolar analog core operates from 5-V and 3.3-V supplies, while the output uses a 3.3-V supply to provide LVDS-compatible outputs. Prior to the track-and-hold, the analog input signal passes through a high-performance bipolar buffer. The buffer presents a high and consistent impedance to the analog inputs. The buffer isolates the board circuitry external to the ADC from the sampling glitches caused by the track-and-hold in the ADC. The conversion process is initiated by the falling edge of the external input clock. At that instant, the differential input signal is captured by the input track-and-hold, and the input sample is converted sequentially by a series of lower resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 4.5 clock cycles, after which the output data are available as a 16-bit parallel word, coded in offset binary format.

Input Configuration

The analog input for the ADS548x consists of an analog pseudo-differential buffer followed by a bipolar transistor T & H. The analog buffer isolates the source driving the input of the ADC from any internal switching and presents a high impedance to drive at high input frequencies, as compared to an ADC without a buffered input. The input common-mode is set internally through a 1000-Ω resistor connected from 3.1 V to each of the inputs. This configuration results in a differential input impedance of 2 kΩ at 0 Hz. Figure 30 estimates the package parasitics before soldering to a board. Each board is different, but soldering to the board will likely add 1 – 2 pF to the input capacitance.

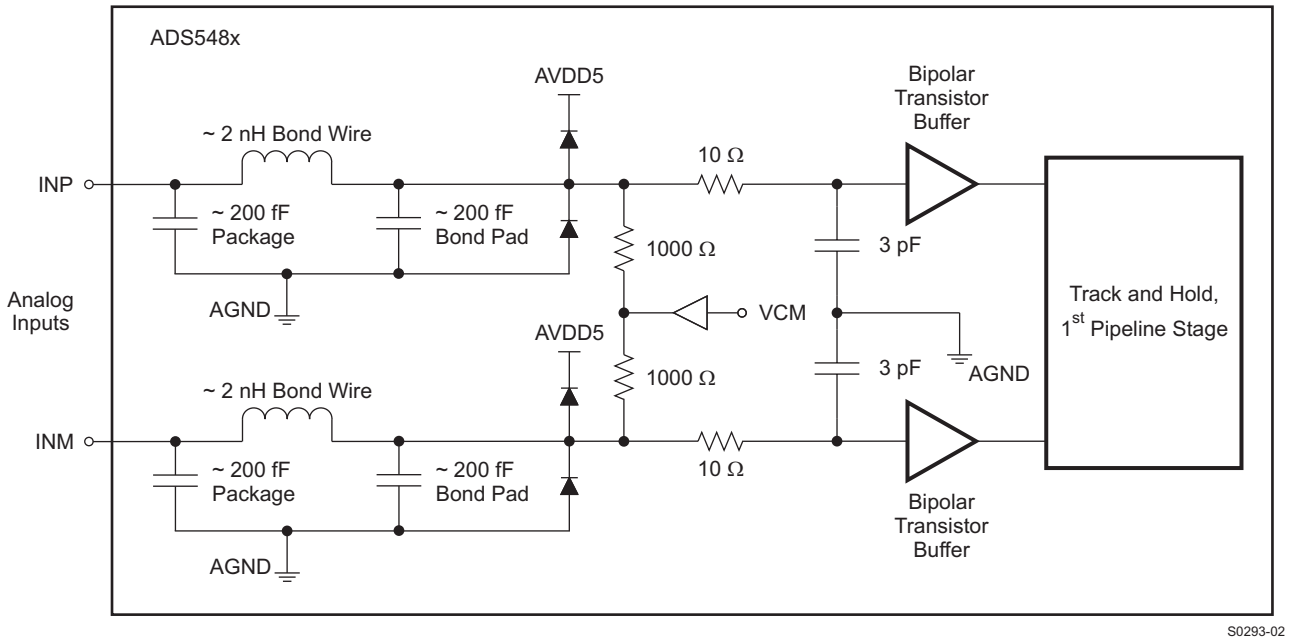


Figure 30. Analog Input Circuit (unsoldered package)

For a full-scale differential input, each of the differential lines of the input signal (pins 11 and 12) swings symmetrically between (3.1 V + 0.75 V) and (3.1 V – 0.75 V). This range means that each input has a maximum signal swing of 1.5 V_{PP} for a total differential input signal swing of 3 V_{PP}. Operation below 3 V_{PP} is allowable, with the characteristics of performance versus input amplitude demonstrated in Figure 8 through Figure 10. For instance, for performance at 2 V_{PP} rather than 3 V_{PP}, refer to the SNR and SFDR at –3.5 dBFS (0 dBFS =

3 V_{PP}). The maximum swing is determined by the internal reference voltage generator, eliminating the need for any external circuitry for this purpose. The primary degradation visible if the maximum amplitude is kept to 2 V_{PP} is ~3 dBc of SNR compared to using 3 V_{PP}, while SFDR is the same or even improved. The smaller input signal also possibly helps any components in the signal chain prior to the ADC to be more linear and provide better distortion.

The ADS548x performs optimally when the analog inputs are driven differentially. The circuit in Figure 31 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. If voltage gain is required, a step-up transformer can be used.

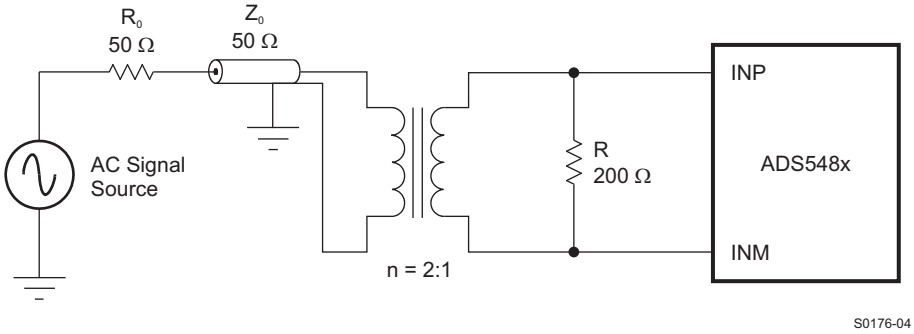


Figure 31. Converting a Single-Ended Input to a Differential Signal Using an RF Transformer

Dither

The ADS548x family of devices contain a dither option that is enabled via the DITHEREN pin. Dither is a technique applied to convert small static errors in the converter to dynamic errors, which look similar to white noise in the output. It improves the harmonics that are a function of the static errors. The dither is a low level and is only indicated in the output waveform as wideband noise that may slightly degrade the SNR. It is recommended that users should allow the capability to enable/disable it in the event they would like to compare the results during their evaluation. In addition to the plots on the first page of the data sheet, Figure 8 through Figure 10 and Figure 19 through Figure 21 show the minor differences of dither on/off when studied.

External Voltage Reference

For systems that require the analog signal gain to be adjusted or calibrated, this can be performed by using an external reference. The dependency on the signal amplitude to the value of the external reference voltage is characterized typically by Figure 32 (VREF = 1.2 V is normalized to 0 dB as this is the internal reference voltage). As can be seen in the linear fit, this equates to approximately ~1 dB of signal adjustment per 100 mV of reference adjustment. The range of allowable variation depends on the analog input amplitude that is applied to the inputs and the desired spectral performance, as can be seen in the performance versus external reference graphs in Figure 33 and Figure 34.

For dc-coupled applications that use the VCM pin of the ADS548x as the common mode of the signal in the analog signal gain path prior to the ADC inputs, Figure 36 indicates little change in VCM output as VREF is externally adjusted. The VCM output is buffered with a 2-kΩ series output resistor.

The method for disabling the internal reference for use with an external reference is described in Table 4 . The following VREF adjustment graphs were collected using the ADS5483, but are indicative of the behavior of the ADS5484/5485. The absolute performance may differ from device to device, but the relative characteristics are valid.

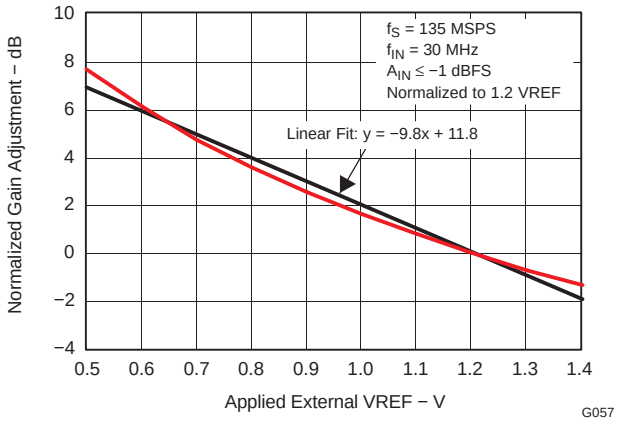


Figure 32. Signal Gain Adjustment versus External Reference (VREF)

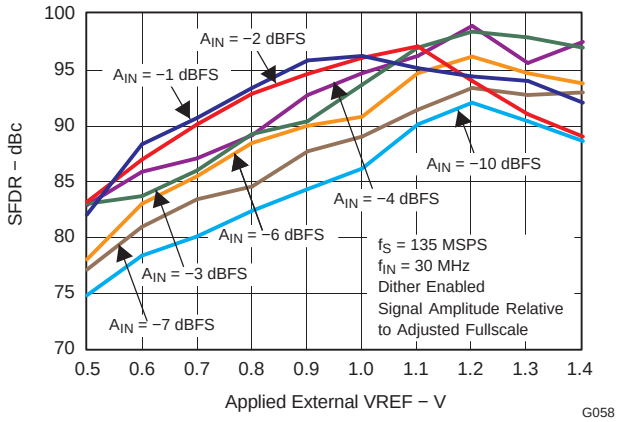


Figure 33. SFDR versus External VREF and A_{IN}

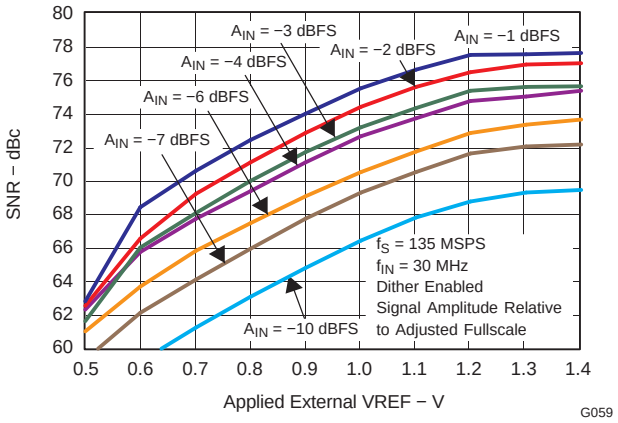


Figure 34. SNR versus External VREF and A_{IN}

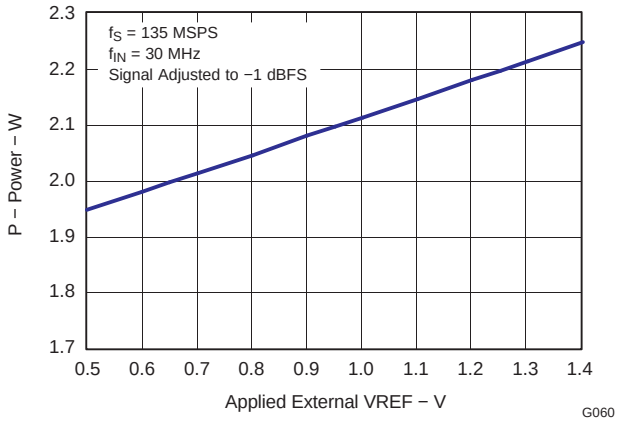


Figure 35. Total Power Consumption versus External VREF

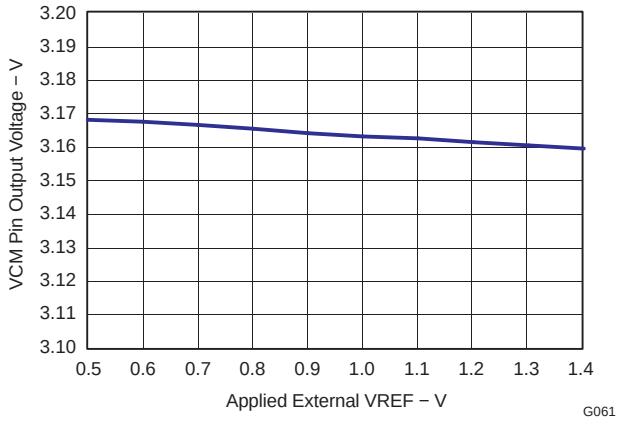


Figure 36. VCM Pin Output versus External VREF

Clock Inputs

The ADS548x equivalent clock input circuit is shown in Figure 37. The clock inputs can be driven with either a differential clock signal or a single-ended clock input, but differential is highly recommended. The characterization of the ADS548x is typically performed with a 3-V_{PP} differential clock, but the ADC performs well with a differential clock amplitude down to ~1 V_{PP}, as shown in Figure 39 and Figure 40 . The performance is optimized when the clock amplitude is kept above 2 V_{PP}. The clock amplitude becomes more of a factor in performance as the analog input frequency increases. When single-ended clocking is a necessity, it is best to connect CLKM to ground with a 0.01-µF capacitor, while CLKP is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 38.

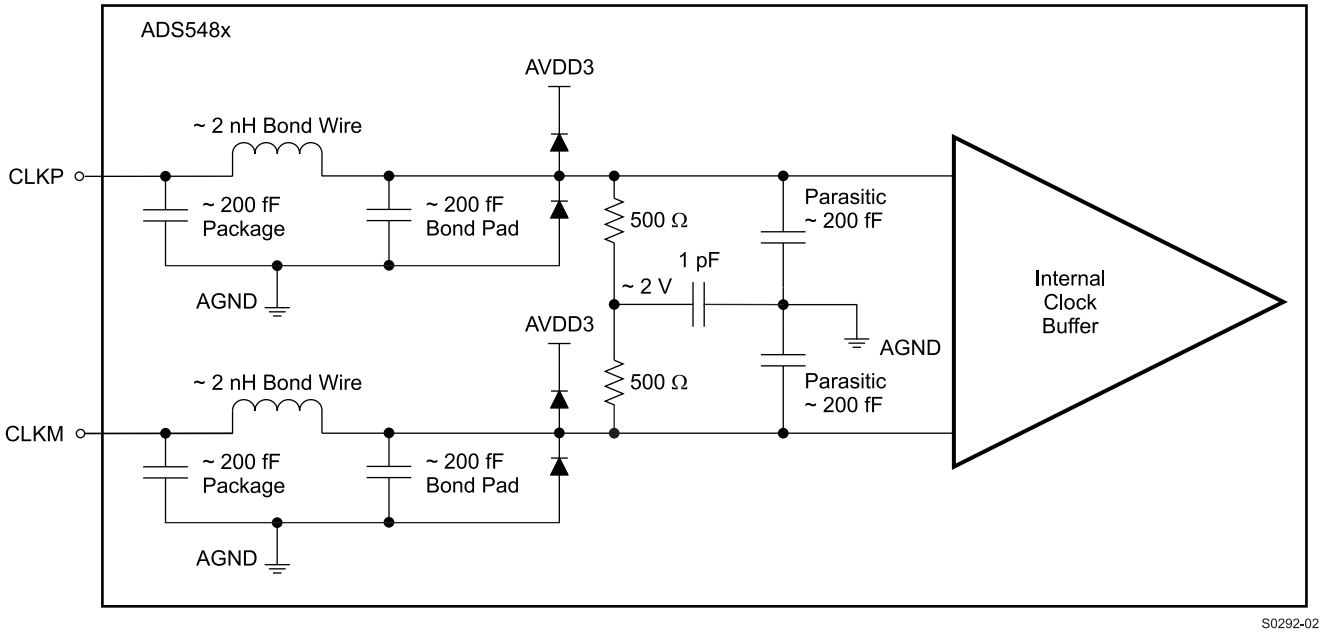


Figure 37. Clock Input Circuit

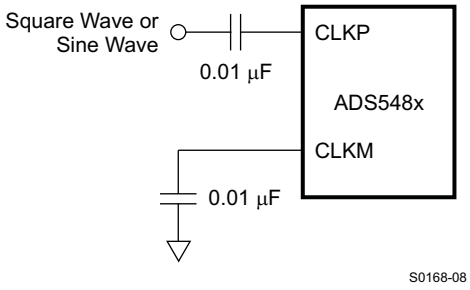


Figure 38. Single-Ended Clock

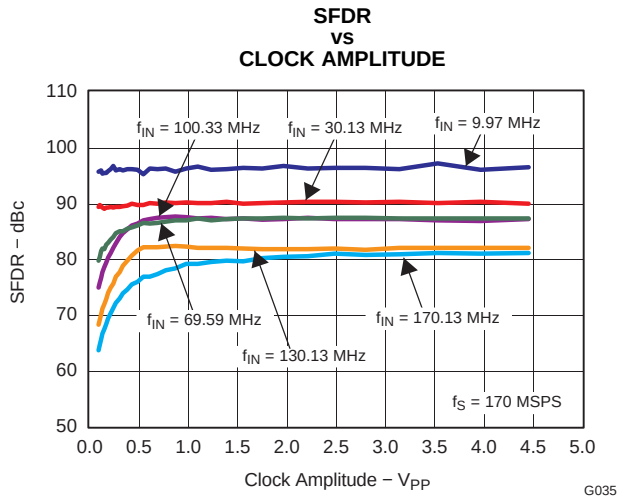


Figure 39.

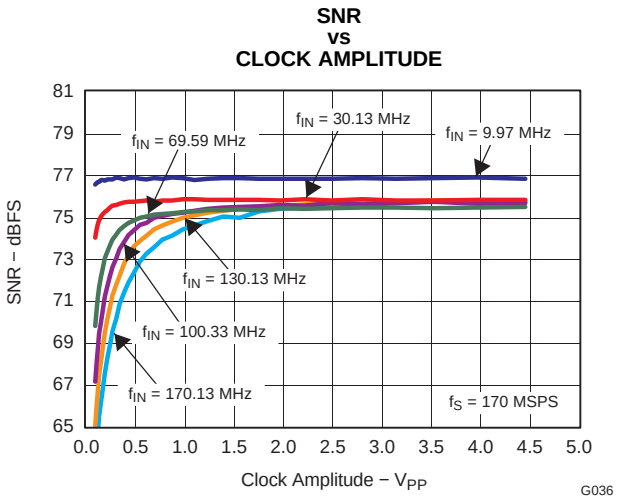


Figure 40.

For jitter-sensitive applications, the use of a differential clock has some advantages at the system level. The differential clock allows for common-mode noise rejection at the printed circuit board (PCB) level. With a differential clock, the signal-to-noise ratio of the ADC is better for jitter-sensitive, high-frequency applications because the board level clock jitter is superior.

The sampling process is more sensitive to jitter using high analog input frequencies or slow clock frequencies. Large clock amplitude levels are recommended when possible to reduce the indecision (jitter) in the ADC clock input buffer. Whenever possible, the ideal combination is a differential clock with large signal swing (~1 – 3 V_{PP}). Figure 41 demonstrates a recommended method for converting a single-ended clock source into a differential clock; it is similar to the configuration found on the evaluation board and was used for much of the characterization. See also *Clocking High Speed Data Converters* (SLYT075) for more details.

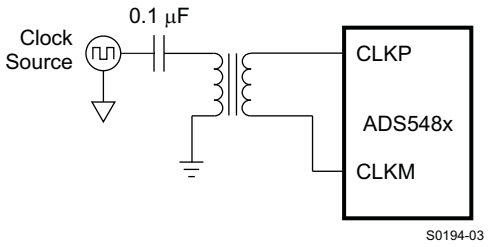


Figure 41. Differential Clock

The common-mode voltage of the clock inputs is set internally to ~2 V using internal 0.5-kΩ resistors. It is recommended to use ac coupling, but if this scheme is not possible, the ADS548x features good tolerance to clock common-mode variation (as shown in Figure 42 and Figure 43). The internal ADC core uses both edges of the clock for the conversion process. Ideally, a 50% duty-cycle clock signal should be provided. Performance degradation as a result of duty cycle can be seen in Figure 44.

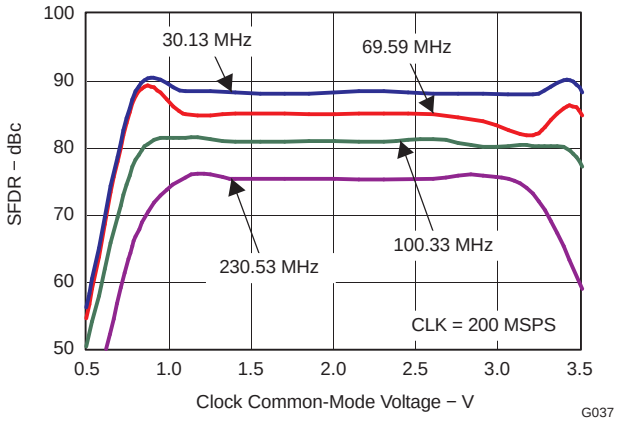


Figure 42. SFDR versus Clock Common-Mode Voltage

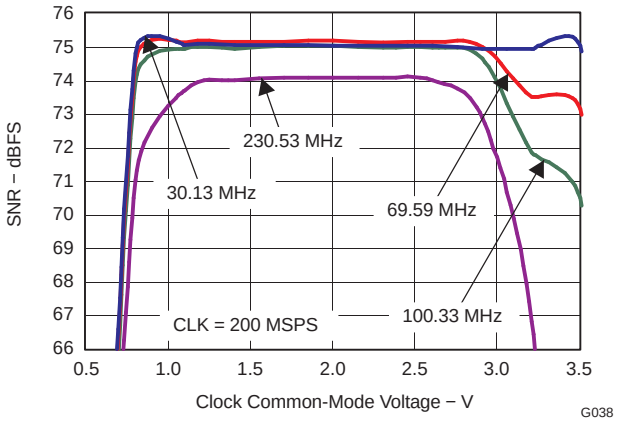


Figure 43. SNR versus Clock Common-Mode Voltage

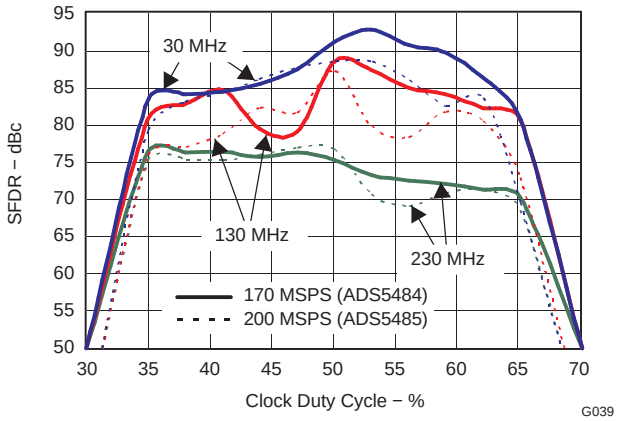


Figure 44. SFDR vs Clock Duty Cycle

The ADS5484 is capable of achieving 75.7 dBFS SNR at 130 MHz of analog input frequency. In order to achieve the SNR at 130 MHz the clock source rms jitter (at the ADC clock input pins) must be at most 184 fsec in order for the total rms jitter to be 201 fsec due to internal ADC aperture jitter of ~80 fsec. A summary of maximum recommended rms clock jitter as a function of analog input frequency for the ADS5484 is provided in Table 2. The equations used to create the table are presented and can be used to estimate required clock jitter for virtually any pipeline ADC, but in particular, the ADS5481/5482/5483/5484/5485 family.

Table 2. Recommended Approximate RMS Clock Jitter for ADS5484

ANALOG INPUT FREQUENCY (MHz)	MEASURED SNR (dBc)	TOTAL JITTER (fsec rms)	MAXIMUM CLOCK JITTER (fsec rms)
10	76.8	2301	2299
30	75.9	851	847
70	75.7	373	364
130	75.7	201	184
170	75.6	155	133
230	74.9	124	95

Equation 1 and Equation 2 are used to estimate the required clock source jitter.

$$SNR\ (dBc) = -20 \times LOG10\ (2 \times \pi \times f_{IN} \times j_{TOTAL}) \quad (1)$$

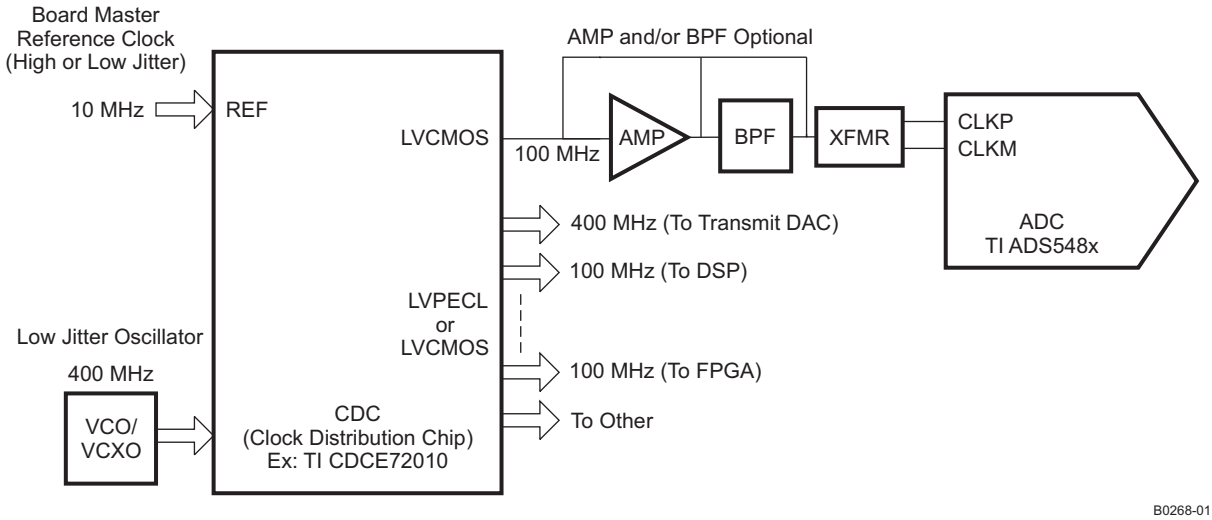
$$j_{TOTAL} = (j_{ADC}^{2} + j_{CLOCK}^{2})^{1/2} \quad (2)$$

where:

j_{TOTAL} = the rms summation of the clock and ADC aperture jitter;
j_{ADC} = the ADC internal aperture jitter which is located in the data sheet;
j_{CLOCK} = the rms jitter of the clock at the clock input pins to the ADC; and
f_{IN} = the analog input frequency.

Notice that the SNR is a strong function of the analog input frequency, not the clock frequency. The slope of the clock source edges can have a mild impact on SNR as well and is not taken into account for these estimates. For this reason, maximizing clock source amplitudes at the ADC clock inputs is recommended, though not required (faster slope is desirable for jitter-related SNR). For more information on clocking high-speed ADCs, see Application Note SLWA034, *Implementing a CDC7005 Low Jitter Clock Solution For High-Speed, High-IF ADC Devices*, on the Texas Instruments web site. Recommended clock distribution chips (CDCs) are the TI CDCE72010 and CDCM7005. Depending on the jitter requirements, a band pass filter (BPF) is sometimes required between the CDC and the ADC. If the insertion loss of the BPF causes the clock amplitude to be too low for the ADC, or the clock source amplitude is too low to begin with, an inexpensive amplifier can be placed between the CDC and the BPF, as its harmonics and wide-band noise are reduced by the BPF.

Figure 45 represents a scenario where an LVCMOS single-ended clock output is used from a TI CDCE72010 with the clock signal path optimized for maximum amplitude and minimum jitter. The jitter of this setup is difficult to estimate and requires a careful phase noise analysis of the clock path. The BPF (and possibly a low-cost amplifier because of insertion loss in the BPF) can improve the jitter between the CDC and ADC when the jitter provided by the CDC is still not adequate. The total jitter at the CDCE72010 output depends largely on the phase noise of the VCXO/VCO selected, as well as from the CDCE72010 itself.



Consult the CDCE72010 data sheet for proper schematic and specifications regarding allowable input and output frequency and amplitude ranges.

Figure 45. Optimum Jitter Clock Circuit

Digital Outputs

The ADC provides eight LVDS-compatible, offset binary, DDR data outputs (2 bits per LVDS output driver) and a data-ready LVDS signal (DRY). It is recommended to use the DRY signal to capture the output data of the ADS548x (use as a clock output). DRY is source-synchronous to the DATA outputs and operates at the same frequency, creating a full-rate DDR interface that updates data on both the rising and falling edges of DRY. It is recommended that the capacitive loading on the digital outputs be minimized. Higher capacitance shortens the data-valid timing window. The values given for timing (see Figure 1) were obtained with a 5-pF parasitic board capacitance to ground on each LVDS line. When setting the time relationship between DRY and DATA at the receiving device, it is generally recommended that setup time be maximized, but this partially depends on the setup and hold times of the device receiving the digital data. Since DRY and DATA are coincident, it will likely be necessary to delay either DRY such that DATA setup time is maximized.

The LVDS outputs all require an external 100-Ω load between each output pair in order to meet the expected LVDS voltage levels. For long trace lengths, it may be necessary to place a 100-Ω load on each digital output as close to the ADS548x as possible and another 100-Ω differential load at the end of the LVDS transmission line to terminate the transmission line and avoid signal reflections. The effective load in this case reduces the LVDS voltage levels by half. The current of all LVDS drivers is set externally with a resistor connected between the LVDSB (LVDS bias) pin and ground. Normal LVDS current is 3.5 mA per LVDS pair, set with a 10-kΩ external resistor. For systems with excessive load capacitance on the LVDS lines, reducing the resistor value in order to increase the LVDS bias current is allowed to create a stronger LVDS drive capability. For systems with short traces and minimal loading, increasing the resistor in order to decrease the LVDS current is allowable in order to save power. Table 3 provides a sampling of LVDSB resistor values should deviation from the recommended LVDS output current of 3.5 mA be considered. It is not recommended to exceed the range listed in the table. If the LVDS bias current is adjusted, the differential load resistance should also be adjusted to maintain voltage levels within the specification for the LVDS outputs. The signal integrity of the LVDS lines on the board layout should be scrutinized to ensure proper LVDS signal integrity exists.

Table 3. Setting the LVDS Current Drive

LVDSB RESISTOR TO GND, Ω	LVDS NOMINAL CURRENT, mA
6k	5.6
8k	4.3
10k (value for normal recommended operation)	**3.5**
12k	2.8
14k	2.3
16k	2.0
18k	1.7
20k	1.5

Power Supplies and Sleep Modes

The ADS548x uses three power supplies. For the analog portion of the design, a 5-V and 3.3-V supply (AVDD5 and AVDD3) are used, while the digital portion uses a 3.3-V supply (DVDD3). The use of low-noise power supplies with adequate decoupling is recommended. Linear supplies are preferred to switched supplies; switched supplies generate more noise that can be coupled to the ADS548x. However, the PSRR value and plot shown in Figure 46 were obtained without bulk supply decoupling capacitors. When bulk (0.1-µF) decoupling capacitors are used near the supply pins, the board-level PSRR is much higher than the stated value for the ADC. The user may be able to supply power to the device with a less-than-ideal supply and still achieve good performance. It is not possible to make a single recommendation for every type of supply and level of decoupling for all systems. If the noise characteristics of the available supplies are understood, a study of the PSRR data for the ADS548x may provide the user with enough information to select noisy supplies if the performance is still acceptable within the frequency range of interest. The power consumption of the ADS548x does not change substantially over clock rate or input frequency.

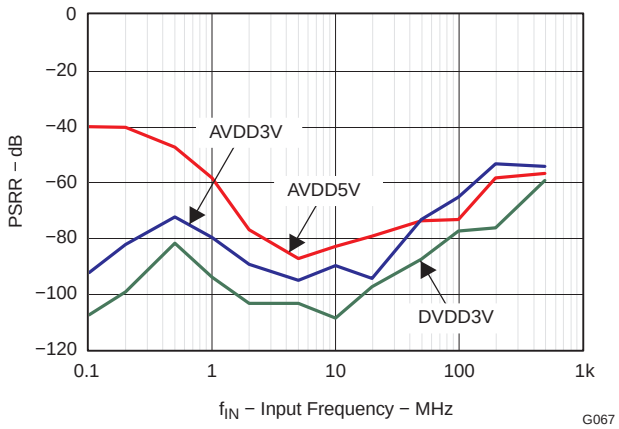


Figure 46. PSRR versus Supply Injected Frequency

Two separate sleep modes are offered. They are differentiated by the amount of power consumed and the time it takes for the ADC to wake-up from sleep. The light sleep mode consumes 605 mW and can be used when wake-up of less than 600 µs is required. Deep sleep consumes 70 mW and requires 6 ms to wake-up. See the wake-up characteristic in Figure 27. For directions on enabling these modes, see Table 4. The input clock can be in either state when the power-down modes are enabled. The device can enter power-down mode whether using an internal or external reference. However, the wake-up time from light sleep enabled to external reference mode is dependent on the external reference voltage and is not necessarily 0.6 ms, but should be noticeably faster than deep sleep wake-up. No specific power sequences are required.

Table 4. Power-Down and Reference Modes

MODE	PDWNF PIN	PDWNS PIN	POWER CONSUMPTION	WAKE-UP TIME
ADC On - Internal reference	Low	Low	2.16 W	On
ADC On - External reference	High	High	2.16 W	On
Light sleep	High	Low	600 mW when enabled	0.6 ms
Deep sleep	Low	High	70 mW when enabled	6 ms

Layout Information

The evaluation board represents a good model of how to lay out the printed circuit board (PCB) to obtain the maximum performance from the ADS548x. Follow general design rules, such as the use of multilayer boards, a single ground plane for ADC ground connections, and local decoupling ceramic chip capacitors. The analog input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. The clock signal traces should also be isolated from other signals, especially in applications such as high IF sampling where low jitter is required. Besides performance-oriented rules, care must be taken when considering the heat dissipation of the device. The thermal heat sink included on the bottom of the package should be soldered to the board as described in the *PowerPad Package* section. See the *ADS548x EVM User Guide* on the TI web site for the evaluation board schematic.

PowerPAD Package

The PowerPAD package is a thermally-enhanced, standard-size IC package designed to eliminate the use of bulky heat sink and slugs traditionally used in thermal packages. This package can be easily mounted using standard PCB assembly techniques and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This pad design provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heat sink.

Assembly Process

1. Prepare the PCB top-side etch pattern including etch for the leads as well as the thermal pad as illustrated in the Mechanical Data section (at the end of this data sheet).
2. Place a 6-by-6 array of thermal vias in the thermal pad area. These holes should be 13 mils (0.013 in or 0.3302 mm) in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25 mil (0.025 in or 0.635 mm) diameter holes under the package, but outside the thermal pad area, to provide an additional heat path.
4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via-connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the *PowerPAD Made Easy* application brief (SLMA004) or the *PowerPAD Thermally Enhanced Package* application report (SLMA002), both available for download at www.ti.com.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Duration/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal, expressed as a percentage.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Common-Mode Rejection Ratio (CMRR)

CMRR measures the ability to reject signals that are presented to both analog inputs simultaneously. The injected common-mode frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the CMRR in dB.

Effective Number of Bits (ENOB)

ENOB is a measure in units of bits of converter performance as compared to the theoretical limit based on quantization noise:

ENOB = (SINAD – 1.76)/6.02

Gain Error

Gain error is the deviation of the ADC actual input full-scale range from its ideal value, given as a percentage of the ideal input full-scale range.

Integral Nonlinearity (INL)

INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best-fit line, measured in units of LSB.

Offset Error

Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of the ability to reject frequencies present on the power supply.

The injected frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the PSRR in dB. The measurement calibrates out the benefit of the board supply decoupling capacitors.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and in the first five harmonics.

$$SNR = 10\log_{10}\frac{P_S}{P_N} \quad (4)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10\log_{10}\frac{P_S}{P_N + P_D} \quad (5)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Temperature Drift

Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by $T_{MIN} – T_{MAX}$.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$THD = 10\log_{10}\frac{P_S}{P_D} \quad (6)$$

THD is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3)

IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$). IMD3 is given in units of either dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

PACKAGING INFORMATION

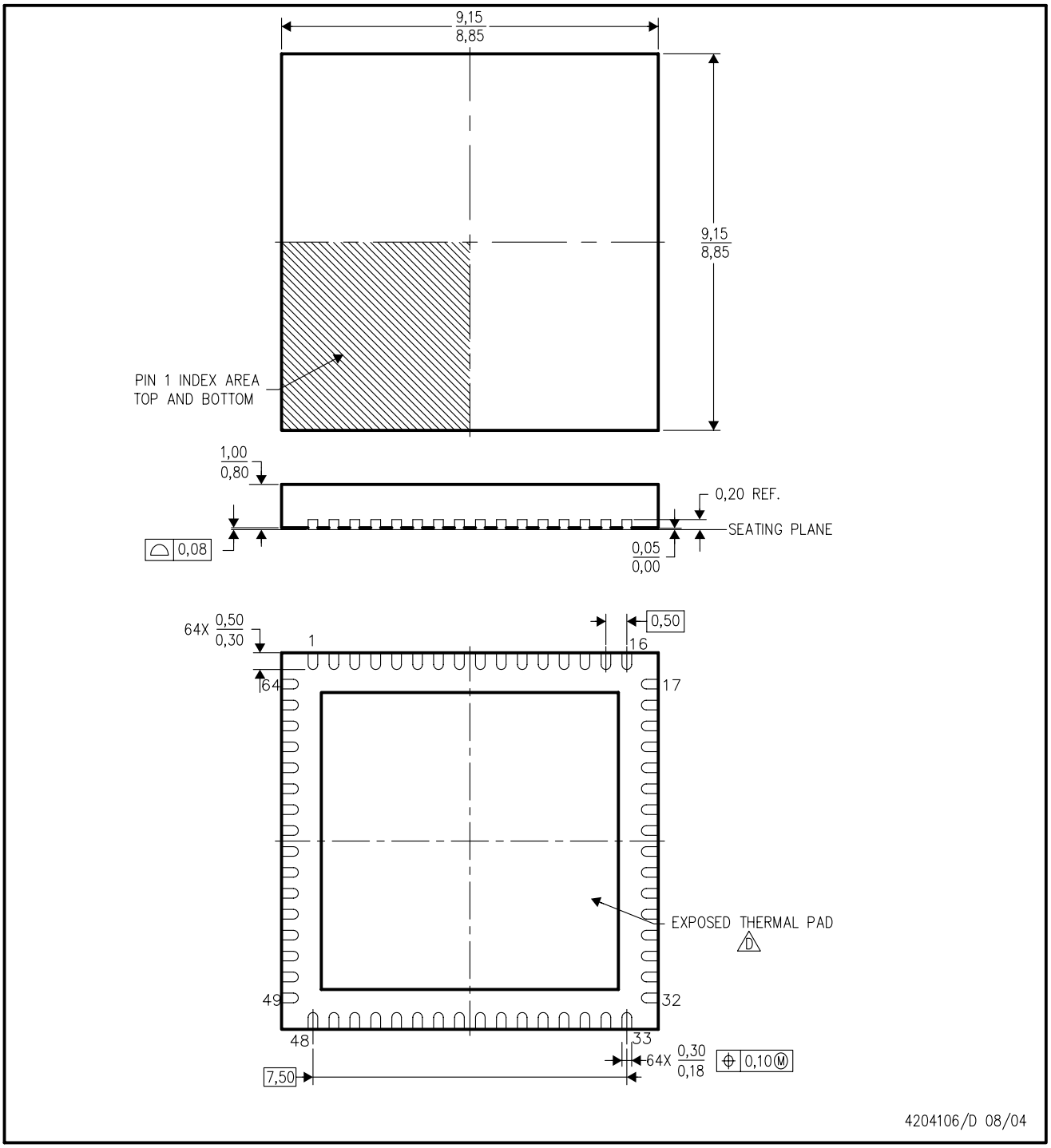
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS5484IRGCR	ACTIVE	VQFN	RGC	64	2000	TBD	Call TI	Call TI
ADS5484IRGCRG4	ACTIVE	VQFN	RGC	64	2000	TBD	Call TI	Call TI
ADS5484IRGCT	ACTIVE	VQFN	RGC	64	250	TBD	Call TI	Call TI
ADS5484IRGCTG4	ACTIVE	VQFN	RGC	64	250	TBD	Call TI	Call TI
ADS5485IRGCR	ACTIVE	VQFN	RGC	64	2000	TBD	Call TI	Call TI
ADS5485IRGCRG4	ACTIVE	VQFN	RGC	64	2000	TBD	Call TI	Call TI
ADS5485IRGCT	ACTIVE	VQFN	RGC	64	250	TBD	Call TI	Call TI
ADS5485IRGCTG4	ACTIVE	VQFN	RGC	64	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGC (S–PQFP–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration .
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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